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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/23/2003

9

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 09/239,898	Applicant(s) SEYYEDY ET AL.	
	Examiner Guy J. Lamarre, P.E.	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41 and 43-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41 and 43-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

0. This office action is in response to Applicants' amendment of 7 July *2003*.

0.1 Claims 1-41, 43-45 remain pending.

0.2 The prior art rejections of record to Claims 1-41, 43-45 stand maintained in response to Applicants' amendment of 7 July *2003*.

Response to Arguments

1. Applicants' arguments of 7 July 2003 have been fully considered, but are not found persuasive.

REMARKS

1.1 In response to claims 1-41, 43-45, on page 15 of the communication, Applicants, citing *In re Vaeck.*, 20 USPQ2d 1438 (Fed. Cir. 1991), assert that the prior art references fail to establish a prima facie basis for rejection under 103. Applicants contend that there is no suggestion or motivation to combine **Matsumura et al.**, **Manning** and **Schober**, and that such suggestion or motivation must be found in the references.

The Examiner disagrees: To establish a prima facie case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. *In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Therefore, such suggestion or motivation may be found not only in the references but also in the knowledge generally available to one of ordinary skill in the art.

Hence, "In determining the propriety of the Patent Office case for obviousness in the first instance, it is necessary to ascertain whether or not the reference teachings would appear to be sufficient for one of ordinary skill in the relevant art having the reference before him to make the

proposed substitution combination, or other modification." *In re Linter*, 458 F.2d 1013, 173 USPQ 560, 562 (CCPA 1972).

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 11192).

The rationale to modify or combine the prior art does not have to be expressly stated in the prior art; the rationale may be expressly or impliedly contained in the prior art or it may be reasoned from knowledge generally available to one of ordinary skill in the art, established scientific principles, or legal precedent established by prior case law. *In re Fine*, 837 F. 2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). See also *In re Eli Lilly & Co.*, 902 F.2d 943. 14 USPQ2d 1741 (Fed. Cir. 1990) (discussion of reliance on legal precedent); *In re Nilssen*, 851 F.2d 1401, 7 USPQ2d 1500, 1502. (Fed. Cir. 1988) (references do not have to explicitly suggest combining teachings); Ex arte Clanp. 227 USPQ 972 (Bd. Pat. App. & Inter. 1985); and Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993) (reliance on logic and sound scientific reasoning).

Also in reference to Ex Varte Levenaood, 28USPQ2d, 1301, the Court stated, "Obviousness is a legal conclusion, the determination of which is a question of patent law. Motivation for combining the teachings of the various references need not be explicitly found in the references themselves, *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). Indeed, the examiner may provide an explanation based on logic and sound scientific reasoning that will support a holding of obviousness. *In re Soli*, 317 F.2d 941, 137 USPQ 797 (CCPA 1963)."

To the extent that the response to the applicant's arguments may have mentioned new portions of the prior art references which were not used in the prior office action, this does not constitute new a new ground of rejection. It is clear that the prior art reference is of record and has been considered entirely by applicant. See *In re Boyer*, 363 F.2d 455, 458 n.2, 150 USPQ 441, 444, n.2 (CCPA 1966) and *In re Bush*, 296 F.2d 491, 496, 131 USPQ 263, 267 (CCPA 1961).

Claim Rejections - 35 USC ' 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2.0 This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

2.1 Claims 1-2, 4-6, 8-10, 12-28, 30-41, and 43-45 are rejected under 35 U.S.C. 103 (a) as being unpatentable over **Matsumura et al.** (US Patent No. 5,991,232; August 28, 1998) in view of **Manning** (US Patent No. 6,032,274; Feb 29, 2000).

As per Claims 1-2, 4-6, 8-10, 12-28, 30-41, 43-45, **Matsumura's** Fig. 23 substantially depicts the claimed compression and testing means for double rate data in "*Logic Block 4j*" including associated structure, synchronization and signal/address controlling means required therefor, such as means for applying voltages and timing stimulus to intermediate nodes, logic gate means (Fig. 19) made of transistor components, data storing or latching means (Latch circuit 4 a, c, e, g, k), timing and signal inverting means as in figs. 7, 28-29, e.g., "*FIG. 21 schematically shows a whole structure of a semiconductor integrated circuit device according to*

an embodiment 3 of the invention. The semiconductor integrated circuit device shown in FIG. 21 differs from the semiconductor integrated circuit device shown in FIG. 13 in the following point. The device is provided with a compression circuit 4j which ***compresses data*** *of 256 bits issued from latch circuit 4e into data of 1 bits, and a latch 4k which transfers and applies a signal of 1 bit from compression circuit 4j to a pad 8p in accordance with* ***test clock signal*** *ETCLK. Structures other than the above are the same as those shown in FIG. 13."* **Not specifically described** in detail in **Matsumura et al.** is the step whereby compressed data is output on edges of a clock. **However** such approach is well known, e.g., **Manning,** in an analogous art, discloses a "*Method and apparatus for compressed data testing of more than one memory array,"* wherein such techniques are described. {See **Manning,** Id., wherein "*Responsive to the test read command, each of the output drivers supplies either data or an error indicator at a unique edge of the respective internal data clock. The test outputs from a plurality of memory devices are provided to the test system at sequential edges of the clock in response to a single command. Compressed test data can thus be read at successive clock edges despite the command requiring a plurality of clock edges,*" at col. 5 line 25 et seq.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in **Matsumura et al.** by including therein data timing means as taught by **Manning,** because such modification would provide the procedure disclosed in **Matsumura et al.** with a technique whereby "*Compressed test data can thus be read at successive clock edges despite the command requiring a plurality of clock edges* " to thereby double data transfer rate. {See **Manning,** col. 5 line 25 et seq.}

2.2 Claims 3, 7, 11 and **29** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Matsumura et al.** (US Patent No. 5,991,232; August 28, 1998) in view of **Manning** (US Patent No. 6,032,274; Feb 29, 2000) in further view of **Schober** (US Patent No. 6,297,668; October 2, 2001; Nov. 25, 1998).

As per Claims 3, 7, 11, 29, Manning and Matsumura et al. substantially disclose, in Fig. 23, the claimed compression and testing means for data in "*Logic Block 4j*" including associated structure, synchronization and signal/address controlling means required therefor, such as means for applying voltages and timing stimulus to intermediate nodes, logic gate means (Fig. 19) made of transistor components, data storing or latching means. {See **Matsumura et al.,** Abstract, wherein apparatus and method are described.} **Not specifically described** in detail in **Manning and Matsumura et al.** is the step whereby a structure consisting of pull-up transistors and pull-down transistors is used in data latching. **However** such approach is well known, e.g., **Schober,** in an analogous art, discloses a "*Serial device compaction for improving integrated circuit layouts,*" wherein such techniques are described. {See **Schober,** Id., col. 9 line 35 et seq.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in **Manning** and **Matsumura et al.** by including therein data stabilizer means made up of a network of pull-up transistors and pull-down transistors as taught by **Schober,** because such modification would provide the procedure disclosed in **Manning** and **Matsumura et al.** with a technique whereby "*The active pull-up branch of the slave latch output is reduced from the normal two or more series devices to a single pull-up device. To balance this drive strength, two series pull-down devices are used. To accomplish this, the normal pull-up series devices are moved from the output gate back into the clock inverter. The similar device from the master latch is also pulled into the clock inverter, where they become the same device. In this way, the inverted clock signal is eliminated, resulting in a flip-flop with a single-phase clock that has its race hazard with the master latch output eliminated. Through this technique, slow clocks incurred in very low voltage operation, or for other reasons, do not cause an error in*

flip-flop operation. ***This operation is race-free and this class of flip-flops is therefore called "race-free".*** " {See **Schober,** col. 10 line 48 et seq.}

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

3.0 THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

3.1 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to:

(703) 746-7238, (for After-Final communications),

(703) 746-7239, (for formal communications intended for entry),

(703) 746-5463 (for informal or draft communications, please label "PROPOSED" or "DRAFT").

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (703) 305-0755. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached on (703) 305-9595.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900

Guy J. Lamarre, P.E.

Guy J. Lamarre

Patent Examiner

9/16/03

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